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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,442	03/01/2006	Mun-Pyo Hong	PNK-0242	7000
23413 7590 12/12/2008 CANTOR COLBURN, LLP 20 Church Street 22nd Floor Hartford, CT 06103				
EXAMINER POMPEY, RON EVERETT				
ART UNIT		PAPER NUMBER		
2812				
NOTIFICATION DATE		DELIVERY MODE		
12/12/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptopatentmail@cantorcolburn.com

Office Action Summary

Application No.

10/531,442

Applicant(s)

HONG ET AL.

Examiner

RON E. POMPEY

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
4a) Of the above claim(s) 5-12 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-4, 13 and 14-15 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/5508)
Paper No(s)/Mail Date 8-1-08
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6624871), in view of Morozumi (US 4862237).

Kim discloses the limitations of:

Claim 1. A thin film transistor array panel comprising:

a gate wire formed on the substrate and including a plurality of gate lines (31L, figs. 3 and 4A) and a plurality of gate electrodes (31G, figs. 3 and 4A) connected to the gate lines;

a gate insulating layer (32, fig. 4A) formed on the gate line;

a semiconductor layer (33, fig. 4A) formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a plurality of data lines (35L, figs. 3 and 4A) intersecting the gate lines, a plurality of source electrodes (35S, figs. 3 and 4A) connected to the data lines, and a plurality of drain electrodes (35D, figs. 3 and 4A) located opposite the source electrodes with respect to the gate electrodes;

a plurality of pixel electrodes (37, figs. 3 and 4A) connected to the drain electrodes; and

an etching assistant pattern (33(under 35P), fig. 4A) made of the same layer as the semiconductor layer (33, fig. 4A) and located out of an area enclosed (out of the area because the pad area is the section of semiconductor layer that is at end of the data line outside the pixel area) by the gate lines and the data lines (col. 4, Ins. 18-25; fig. 3).

Claim 2. The thin film transistor array panel of claim 1, wherein the data wire comprises a lower film of Cr, Mo or Mo ally and an upper film of Al or Al ally (35S/35D/35P/35L, fig. 4A; col. 4, Ins. 28-31).

Claim 3. The thin film transistor array panel of claim 2, further comprising a passivation layer (36, fig. 4A) disposed between the data wire and the pixel electrode.

Claim 4. The thin film transistor array panel of claim 3, wherein the semiconductor layer has substantially the same planar shape as the data wire except for a channel portion located between the data line and the drain electrode (fig. 4A; col. 4, Ins. 18-25).

Claim 13. The thin film transistor array panel of claim 1, wherein the etching assistant pattern is located outside of a pixel area (33(under 35P), figs. 3 and 4A).

Claim 14. The thin film transistor array panel of claim 1, wherein the etching assistant (33(under 35P), fig. 4A) pattern is formed directly on the gate insulating layer (32(under 35P), fig. 4A).

Claim 15. (New) The thin film transistor array panel of claim 1, wherein the thickness of the etching assistant pattern (33(under 35P), fig. 4A) is thinner than a thickness of the semiconductor layer (33(under 35D and 35S), fig. 4A).

3. Kim, as indicated above, discloses all the features of the claims except:

Claim 1: an insulating substrate.

- a. However, Morozumi discloses:

an insulating substrate (col. 6, ln. 66 – col. 7, ln. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the substrate in Kim, with the insulating substrate as taught by Morozumi, because blooming and smear can be avoided.

Response to Arguments

2. Applicant's arguments with respect to claim1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RON E. POMPEY whose telephone number is (571)272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Walter L. Lindsay, Jr./
Primary Examiner, Art Unit 2812

/Ron E Pompey/
Examiner, Art Unit 2812

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